

IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A field effect transistor (FET) comprising:
 - a source region;
 - a drain region;
 - a channel region disposed between the source and drain regions;
 - a bifurcated gate region positioned over said channel region; and
 - a gate oxide layer adjacent to said gate region, wherein said gate oxide layer comprises an alkali metal ion implanted at a dosage calculated based on threshold voltage test data provided by a post silicide electrical test conducted on said FET, and wherein each of said source and drain regions comprise a semiconductor layer comprising said alkali metal ion.
2. (Original) The transistor of claim 1, further comprising:
 - a substrate;
 - an isolation layer positioned over said substrate; and
 - at least one fin structure disposed between the source and drain regions;
 - wherein said source and drain regions are positioned over said isolation layer.
3. (Original) The transistor of claim 1, wherein said alkali metal ion comprises any of cesium and rubidium.

4. (Previously Presented) The transistor of claim 1, wherein said transistor is one of a plurality of transistors comprised by a CMOS (complementary metal oxide semiconductor) device.
5. (Previously Presented) The transistor of claim 4, wherein said plurality of transistors comprises any of a nFET device and a pFET device.
6. (Previously Presented) The transistor of claim 1, wherein an ion implantation level of said alkali metal ion is approximately $3 \times 10^{18} \text{ cm}^{-3}$.
7. (Original) The transistor of claim 1, wherein said gate region comprises silicide.
8. (Previously Presented) The transistor of claim 5, wherein said alkali metal ion adjusts nFET and pFET threshold voltages for the nFET and pFET devices by an amount required to match desired off-currents for said nFET and pFET devices.
9. (Currently Amended) A CMOS (complementary metal oxide semiconductor) device comprising:
 - raised source and drain regions;
 - a channel region disposed between said source and drain regions;
 - a gate region positioned over said channel region;

a silicon layer dividing said gate region; and
a gate oxide layer adjacent to said gate region, wherein said gate oxide layer comprises an alkali metal ion implanted at a dosage calculated based on threshold voltage test data provided by a post silicide electrical test conducted on said CMOS device, and wherein each of said source and drain regions comprise a semiconductor layer comprising said alkali metal ion.

10. (Previously Presented) The device of claim 9, further comprising:
a substrate;
an isolation layer positioned over said substrate; and
at least one fin structure disposed between said source and drain regions;
wherein said source and drain regions are positioned over said isolation layer.
11. (Original) The device of claim 9, wherein said alkali metal ion comprises any of cesium and rubidium.
12. (Previously Presented) The device of claim 9, further comprising a plurality of FET (field effect transistor) devices, wherein said plurality of FET devices comprises any of a nFET device and a pFET device.
13. (Previously Presented) The device of claim 9, wherein an ion implantation level of said alkali metal ion is approximately $3 \times 10^{18} \text{ cm}^{-3}$.

14. (Previously Presented) The device of claim 9, further comprising spacers separating said gate region from said source and drain regions.

15. (Original) The device of claim 9, wherein said gate region comprises silicide.

16. (Previously Presented) The device of claim 12, wherein said alkali metal ion adjusts nFET and pFET threshold voltages for the nFET and pFET devices by an amount required to match desired off-currents for said nFET and pFET devices.

17-23. (Canceled).

24. (Previously Presented) The transistor of claim 1, further comprising spacers separating said gate region from said source and drain regions.

25. (Cancelled).

26. (Previously Presented) The transistor of claim 2, wherein said dosage of the alkali metal ion implantation is a function of a height of said fin structure divided by a thickness of said gate oxide multiplied by a calculated dosage level of said alkali metal ion implanted in a direction normal to said channel region.

27. (Previously Presented) The transistor of claim 1, further comprising a silicide on said source and drain regions.
28. (Cancelled).
29. (Previously Presented) The device of claim 10, wherein said dosage of the alkali metal ion implantation is a function of a height of said fin structure divided by a thickness of said gate oxide multiplied by a calculated dosage level of said alkali metal ion implanted in a direction normal to said channel region.
30. (Previously Presented) The device of claim 9, further comprising a silicide on said source and drain regions.

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6